

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 100353-00185	SERIAL NO. 10/808,532 Unknown
LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT TACHIBANA, et al.	
		FILING DATE March 25, 2004	GROUP 2838 Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO PART.		
BT	AF	05-204479	August 13, 1993	Japan					X
	AG	06-309052	November 4, 1994	Japan					X
	AH	08-186484	July 16, 1996	Japan					X
	AI	10-198447	July 31, 1998	Japan					X
	AJ	2001-147725	May 29, 2001	Japan					X
	AK	2002-99336	April 5, 2002	Japan					X
BT	AL	2003-78366	March 14, 2003	Japan					X

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

BT	AM	G. Tzanateas, C.A.T. Salama, and Y.P. Tsvividis, "A CMOS Bandgap Voltage Reference," IEEE Journal of Solid-State Circuits, Vol. SC-14, No. 3, pp. 655-657, June 1979
	AN	K.N. Leung, and P. K. T. Mok, "A Sub-1-V 15-ppm/°C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Devices," IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, pp. 526-530, April 2002
	AO	A. Boni, "Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply," IEEE Journal of Solid-State Circuits, Vol. 37, No. 10, pp. 1339-1343, October 2002
BT	AP	H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, pp. 670-674, May 1999

EXAMINER Ba Va	DATE CONSIDERED 6-21-2005
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	